IN THE CLAIMS:

Claims 1, 5, 20, 22-30, 33-36 and 38 have been amended herein. All of the pending claims 1 through 38 are presented below. This listing of claims will replace all prior versions and listings of claims in the application. Please enter these claims as amended.

Listing of Claims:

1. (currently amended) A drying system for a semiconductor structure comprising:

a vessel having a top, a bottom, and a plurality of at least three sides ~~forming a vessel~~, the vessel including a semiconductor stage for disposing the semiconductor structure thereon;

a DI water inlet configured to supply DI water in the vessel to at least partially fill the vessel to a level that would allow the semiconductor structure disposed on the semiconductor stage to be submerged in the DI water;

at least one gas inlet configured to supply a gas inert to the semiconductor structure to substantially fill the vessel so that the gas is maintained above the level of the DI water, the at least one gas inlet connected to a fail-shut valve, the at least one gas inlet comprising one of an inlet in the top of the vessel and an inlet ~~in the~~ in at least one side of the at least three sides of the vessel; and

a plurality of liquid inlets configured to supply a liquid to the vessel so that the liquid is disposed between the DI water and the gas, the vessel configured such that the semiconductor stage having the semiconductor structure disposed thereon and an upper surface of the DI water move relative to each other so that the semiconductor structure is exposed through the upper surface of the DI water to the gas to rinse and dry the semiconductor structure in the vessel.

2. (original) The system of claim 1, wherein the vessel includes a plurality of outlets therefrom.

3. (previously presented) The system of claim 1, further comprising:

at least one outlet in the vessel for allowing the gas or DI water to be removed from the vessel; and

a fail-shut valve connected to the at least one outlet in the vessel.

4. (original) The system of claim 1, further comprising at least one outlet in the bottom of the vessel.

5. (currently amended) The system of claim 1, further comprising at least one outlet ~~in the~~ in at least one side of the at least three sides of the vessel.

6. (original) The system of claim 1, wherein the vessel comprises a plurality of weirs.

7. (original) The system of claim 1, wherein the vessel includes a plurality of compartments therein.

8. (original) The system of claim 1, wherein the vessel includes a plurality of compartments therein for allowing flow of liquid in the vessel from one compartment to an adjacent compartment.

9. (original) The system of claim 7, further comprising:

at least one outlet connected to each compartment of the plurality of compartments of the vessel.

10. (original) The system of claim 1, further comprising a rinsing apparatus having at least one spray nozzle with a portion thereof located in the vessel.

11. (original) The system of claim 1, wherein the vessel includes a shelf therein located above the bottom of the vessel.

12. (original) The system of claim 11, wherein the shelf includes at least one aperture therein.

13. (original) The system of claim 1, further comprising:
a valve apparatus connected to at least one liquid inlet of the plurality of liquid inlets.

14. (original) The system of claim 1, wherein the vessel comprises a dry etcher.

15. (original) The system of claim 1, wherein the vessel comprises a cascade rinser.

16. (original) The system of claim 1, wherein the vessel comprises an overflow rinser.

17. (original) The system of claim 1, wherein the vessel comprises a Marangoni dryer.

18. (previously presented) The system of claim 1, wherein the semiconductor stage is raisable so that the semiconductor structure is drawn through the upper surface of the DI water to the gas.

19. (previously presented) The system of claim 1, wherein the vessel comprises at least one drain to lower the upper surface of the DI water to facilitate exposing the semiconductor structure to the gas.

20. (currently amended) A system for a semiconductor structure comprising:

a multi-sided vessel having a top and a bottom, the multi-sided vessel including a semiconductor stage for disposing the semiconductor structure thereon;

a DI water inlet configured to supply DI water in the multi-sided vessel to at least partially fill the multi-sided vessel to a level that would allow the semiconductor structure disposed on the semiconductor stage to be submerged in the DI water;

at least one gas inlet configured to supply a gas inert to the semiconductor structure to substantially fill the multi-sided vessel so that the gas is maintained above the level of the DI water, the at least one gas inlet connected to a fail-shut valve, the at least one gas inlet comprising one of an inlet in the top of the multi-sided vessel and an inlet ~~in the~~ in at least one side of the multi-sided vessel; and

a plurality of liquid inlets configured to supply a liquid to the multi-sided vessel so that the liquid is disposed between the DI water and the gas, the multi-sided vessel configured such that the semiconductor stage having the semiconductor structure disposed thereon and an upper surface of the DI water move relative to each other so that the semiconductor structure is exposed through the upper surface of the DI water to the gas to rinse and dry the semiconductor structure in the multi-sided vessel.

21. (previously presented) The system of claim 20, wherein the vessel includes a plurality of outlets therefrom.

22. (currently amended) The system of claim 20, further comprising:

at least one outlet in the multi-sided vessel for allowing the gas or DI water to be removed from the multi-sided vessel; and

a fail-shut valve connected to the at least one outlet in the multi-sided vessel.

23. (currently amended) The system of claim 20, further comprising at least one outlet in the bottom of the multi-sided vessel.

24. (currently amended) The system of claim 20, further comprising at least one outlet ~~in the~~ in at least one side of the multi-sided vessel.

25. (currently amended) The system of claim 20, wherein the multi-sided vessel comprises a plurality of weirs.

26. (currently amended) The system of claim 20, wherein the multi-sided vessel includes a plurality of compartments therein.

27. (currently amended) The system of claim 20, wherein the multi-sided vessel includes a plurality of compartments therein for allowing flow of liquid in the multi-sided vessel from one compartment to an adjacent compartment.

28. (currently amended) The system of claim 27, further comprising:
at least one outlet connected to each compartment of the plurality of compartments of the multi-sided vessel.

29. (currently amended) The system of claim 20, further comprising a rinsing apparatus having at least one spray nozzle with a portion thereof located in the multi-sided vessel.

30. (currently amended) The system of claim 20, wherein the multi-sided vessel includes a shelf therein located above the bottom of the multi-sided vessel.

31. (previously presented) The system of claim 29, wherein the shelf includes at least one aperture therein.

32. (previously presented) The system of claim 20, further comprising:
a valve apparatus connected to at least one liquid inlet of the plurality of liquid inlets.

33. (currently amended) The system of claim 20, wherein the multi-sided vessel comprises a dry etcher.

34. (currently amended) The system of claim 20, wherein the multi-sided vessel comprises a cascade rinser.

35. (currently amended) The system of claim 20, wherein the multi-sided vessel comprises an overflow rinser.

36. (currently amended) The system of claim 20, wherein the multi-sided vessel comprises a Marangoni dryer.

37. (previously presented) The system of claim 20, wherein the semiconductor stage is raisable so that the semiconductor structure is drawn through the upper surface of the DI water to the gas.

38. (currently amended) The system of claim 20, wherein the multi-sided vessel comprises at least one drain to lower the upper surface of the DI water to facilitate exposing the semiconductor structure to the gas.